

(19) World Intellectual Property
Organization
International Bureau



(43) International Publication Date
20 January 2005 (20.01.2005)

PCT

(10) International Publication Number
WO 2005/006102 A1

(51) International Patent Classification⁷: **G05F 3/24, 3/26**

(21) International Application Number:
PCT/SI2003/000022

(22) International Filing Date: 9 July 2003 (09.07.2003)

(25) Filing Language: English

(26) Publication Language: English

(71) Applicant and

(72) Inventor: **PLETERSEK, Anton** [SI/SI]; Bohova 19c,
2311 Hoce (SI).

CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH,
GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC,
LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW,
MX, MZ, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC,
SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA,
UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States (*regional*): ARIPO patent (GH, GM,
KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW),
Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM),
European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE,
ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO,
SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM,
GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

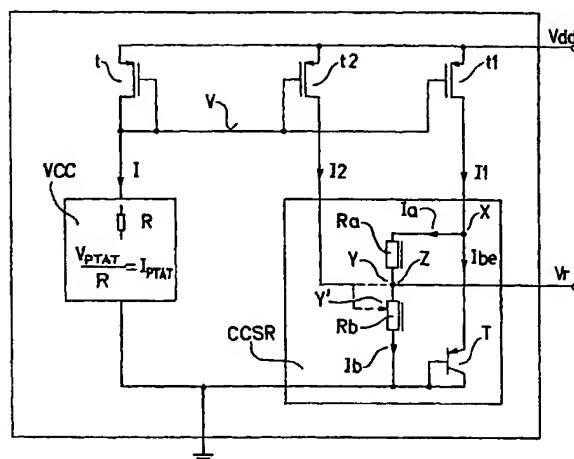
— with international search report

(74) Agent: **PATENTNA PISARNA D.O.O.**; Copova 14, POB
1725, 1001 Ljubljana (SI).

(81) Designated States (*national*): AE, AG, AL, AM, AT, AU,
AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU,

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: **TEMPERATURE INDEPENDENT LOW REFERENCE VOLTAGE SOURCE**



(57) Abstract: A circuit of the invention comprises a low voltage PTAT source. Current generators (t1, t2) are controlled so that their output currents I1 and I2, respectively, have temperature properties of the quotient V_{PTAT}/R . The current I1 is conducted to a first terminal (X) on a first connection of a composition of series connected resistors (Ra, Rb), a second connection thereof being grounded. A transistor (T) is diodelike forward connected between the first terminal (X) and the ground. The current I2 is conducted to a second terminal (Y), preferably being at the same time a common connection (Z) of the resistors (Ra, Rb). Reference voltage Vr is tapped from the connection (Z). Said resistors (Ra, Rb) are manufactured in the n-well technology in the same way as the resistor (R), with the resistance of which the mentioned quotient is generated. The proposed circuit is distinguished for its current controlled summing regulator, which is also suggested by the invention, and which makes it possible that in a temperature range from -50 °C to 150 °C a very low reference voltage of 0.35 V at low supply voltage lying below 0.9 V is reached, and does not simultaneously introduce nonideal behaviour like offset voltage.

WO 2005/006102 A1